

CLAIMS LISTING

1. (Currently Amended) A traffic management processor for processing an unspecified bit rate (UBR) traffic flow and a constant bit rate (CBR) traffic flow, comprising:

a departure time calculator (DTC) circuit for calculating a departure time for each packet received;

a content addressable memory (CAM) device coupled to the DTC circuit and having a plurality of rows, each row including a first portion for storing the departure time for a corresponding packet and including a second portion for storing a CBR bit indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow, wherein an asserted CBR bit indicates the departure time corresponds to a packet of the CBR traffic flow, and a de-asserted CBR bit indicates the departure time corresponds to a packet of the UBR traffic flow; and

compare logic coupled to the CAM device and configured to determine which of the departure times stored in selectively output from the CAM device is the earliest, wherein the CAM device is configured to forward to the compare logic only the departure times having a de-asserted CBR bit so that only the departure times for packets belonging to the UBR traffic flow participate in determining which departure time is the earliest in the compare logic.

2. (Original) The traffic management processor of Claim 1, wherein the packets of the CBR traffic flow and packets of the UBR traffic flow are queued in the same queuing mechanism.

3. (Canceled)

4. (Canceled)

5. (Original) The traffic management processor of Claim 1, wherein the departure times comprise counter values generated by a counter circuit in response to

state transitions of a clock signal.

6. (Original) The traffic management processor of Claim 1, wherein the departure times can be stored in the CAM device in any order, regardless of priority.

7. (Original) The traffic management processor of Claim 1, further comprising a priority encoder coupled to the compare logic.

8. (Original) The traffic management processor of Claim 1, further comprising:

a match line coupled to each row of the CAM device;

a word line coupled to each row of the CAM device; and

means for selectively driving each word line in response to a match condition indicated on the corresponding match line.

9. (Original) The traffic management processor of Claim 1, wherein the compare logic is configured to compare the departure times provided by the CAM device with each other to determine which departure time is the earliest.

10. (Original) The traffic management processor of Claim 9, wherein the CAM device selectively provides the departure times to the compare logic in response to the CBR bits.

11. (Original) The traffic management processor of Claim 10, wherein the departure times corresponding to packets of the CBR traffic flow are not provided to the compare logic.

12. (Original) The traffic management processor of Claim 1, wherein the CAM device further includes an input to receive a current time value.

13. (Original) The traffic management processor of Claim 12, wherein the

CAM device is configured to compare the current time value to only those departure times having an asserted CBR bit.

14. (Original) The traffic management processor of Claim 13, wherein the CAM device is configured to selectively de-assert the CBR bits in response to match conditions in the CAM device.

15. (Original) The traffic management processor of Claim 14, wherein de-assertion of the CBR bit enables the corresponding departure time to participate in determining which departure time is the earliest.

16-21. (Canceled)

22. (Currently Amended) A traffic management processor for simultaneously processing an unspecified bit rate (UBR) traffic flow and a constant bit rate (CBR) traffic flow, comprising:

a departure time calculator (DTC) circuit configured to calculate a departure time for each UBR packet and configured to calculate a departure time window for each CBR packet;

a queuing mechanism coupled to the DTC circuit and configured to queue the UBR packets and the CBR packets together, and further configured to always enable the UBR packets for departure and to selectively enable the CBR packets for departure only if the CBR packet's departure time window comprises a current time value; and

compare logic coupled to the queuing mechanism and configured to compare the departure times for only the packets enabled by the queuing mechanism to select the packets for departure.

23. (Canceled)

24. (Canceled)

25. (Currently Amended) The traffic management processor of Claim 2422, wherein the queuing mechanism comprises a content addressable memory (CAM) device.

26. (Original) The traffic management processor of Claim 25, wherein the CAM device comprises:

a plurality of rows, each row having a first portion for storing the departure time for a corresponding packet and having a second portion for storing a control bit indicating whether the corresponding packet is part of the UBR traffic flow or is part of the CBR traffic flow; and

an input to receive the current time value.

27. (Original) The traffic management processor of Claim 22, wherein the compare logic compares the departure times with each other to determine which of the departure times is the earliest.

28. (Currently Amended) A method of processing a first traffic flow having an unspecified bit rate (UBR) and a second traffic flow having a constant bit rate (CBR), comprising:

calculating a departure time for each packet received;

storing the departure times for packets belonging to all traffic flows in the same table, each departure time having a CBR bit;

asserting the CBR bit for each packet that belongs to the CBR traffic flow;

de-asserting the CBR bit for each packet that belongs to the UBR traffic flow;

determining which of the departure times that have a de-asserted CBR bit is the earliest, wherein only the departure times having de-asserted CBR bits are compared

with each other to determine which departure time is the earliest; and

transmitting the packet corresponding to the earliest departure time.

29. (Canceled)

30. (Original) The method of Claim 28, wherein the table comprises a content addressable memory.

31. (Original) The method of Claim 28, further comprising:  
comparing a current time value with the departure times having asserted CBR bits; and

de-asserting the CBR bit corresponding to the departure time that matches the current time value.

32. (Original) The method of Claim 31, wherein de-asserting the CBR bit enables the corresponding departure time to participate in determining which departure time is the earliest.

33-36. (Canceled)